IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Original) A multistage bit stream multiplexer having a switchable forward/reverse clock relationship comprising:

a first multiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate, wherein the first plurality of bit streams are greater in number than the second plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate, the first multiplexing integrated circuit including:

a phase locked loop (PLL) that receives a reference clock signal and produces a PLL Data Clock having a frequency equal to the second bit rate, and

wherein a plurality of latches receive the PLL Data Clock, latch data multiplexed from the first plurality of bits streams, and produce the second plurality of bit streams;

a second multiplexing integrated circuit that receives the second plurality of bit streams and that outputs at least one high-speed bit stream at a line bit rate that exceeds the second bit rate; and

a clock circuit, wherein the clock circuit generates a forward transmit clock for use by the first multiplexing integrated circuit in producing the second plurality of bit streams based upon a reference clock signal that is selectable from a plurality of inputs based upon a clock selector input, wherein the plurality of inputs include a reverse transmit clock generated by the second multiplexing integrated circuit.

2. (Original) The multistage bit stream multiplexer of claim 1, further comprising:

a communication Application Specific Integrated Circuit (ASIC) from which the first multiplexing integrated circuit receives the first plurality of bit streams; and

a media interface that receives the at least one high-speed bit stream and produces a media output.

3. (Original) The multistage bit stream multiplexer of claim 1, wherein the plurality of inputs further comprises an external oscillator output.

4. (Original) The multistage bit stream multiplexer of claim 1, wherein the plurality of inputs further comprises a voltage controlled oscillator output.

Claims 5-6. (Cancelled)

7. (Currently Amended) The multistage bit stream multiplexer of ~~claim 6~~ claim 1, wherein the frequency of the PLL Data Clock is 16 times the frequency of the reference clock

8. (Original) The multistage bit stream multiplexer of claim 7, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

9. (Original) The multistage bit stream multiplexer of claim 1, wherein the forward transmit clock is a source centered double data rate clock with respect to each of the plurality of second bit streams.

10. (Currently Amended) The multistage bit stream multiplexer of ~~claim 6~~ claim 1, wherein the PLL outputs to the second multiplexing ~~integrated circuit, a~~ integrated circuit a lock detect signal that remains active while the PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference clock signal, and wherein the first multiplexing integrated circuit selects the reverse clock through the clock selector input when the PLL is not locked to the reference clock signal.

11. (Cancelled)

12. (Previously Presented) The multistage bit stream multiplexer of claim 4, wherein the first multiplexing integrated circuit further comprises a phase detector that receives a first input from a loop timing circuit and a second input from one of the plurality of inputs.

13. (Original) The multistage bit stream multiplexer of claim 1, wherein the first multiplexing integrated circuit comprises integrated circuits formed on a silicon substrate and the second multiplexing integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si.

14. (Currently Amended) An upstream multiplexing integrated circuit within a multi-stage bit stream multiplexer that operates with a switchable forward/reverse lock relationship with a downstream multiplexing integrated circuit, comprising:

a plurality of input ports operable to receive a first plurality of bit streams at a first bit rate;

a plurality of output ports to output a second plurality of bit streams at a second bit rate, wherein the first plurality of bit streams is greater in number than the second plurality of bit streams are in number, and wherein the first bit rate is less than the ~~second bit rate; and~~ second bit rate;

a clock circuit that generates a forward transmit clock signal for use by the upstream multiplexing integrated circuit in producing the second plurality of bit streams based upon a reference clock signal selectable from a plurality of inputs, wherein said inputs include a reverse transmit clock generated by the downstream integrated circuit; and

a phase locked loop (PLL) that receives the reference clock signal and produces a PLL Data Clock having a frequency equal to the second bit rate, wherein a plurality of latches receive the PLL Data Clock, latch data multiplexed from the first bit streams and produce the plurality of second bit streams.

15. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the first plurality of bit streams are received from a communication Application Specific Integrated Circuit (ASIC) from which the first multiplexing integrated circuit receives the first plurality of bit streams, and wherein the downstream multiplexing integrated circuit outputs at least one high-speed bit stream to a media interface that produces a media output.

16. (Currently Amended) The upstream multiplexing integrated circuit of claim 14, wherein the plurality of inputs ~~further comprises~~ include an external oscillator output.

17. (Currently Amended) The upstream multiplexing integrated circuit of claim 14, wherein the plurality of inputs ~~further comprises~~ include a voltage-controlled oscillator output.

18. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the reference clock signal is selected based upon a clock selector input.

19. (Cancelled)

20. (Currently Amended) The upstream multiplexing integrated circuit of ~~claim 19~~ claim 14, wherein the frequency of the PLL Data Clock comprises 16 times the frequency of the reference clock.

21. (Currently Amended) The upstream multiplexing integrated circuit of ~~claim 19~~ claim 14, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

22. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the forward transmit clock is a source centered double data rate clock with respect to the second plurality of bit streams.

23. (Currently Amended) The upstream multiplexing integrated circuit of ~~claim 19~~ claim 14, wherein the PLL outputs to ~~the upstream multiplexing integrated circuit, a lock detect signal~~ the upstream multiplexing integrated circuit a lock detect signal that remains active while the PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference clock signal, and wherein the downstream multiplexing integrated circuit selects the ~~reverse clock~~ reverse transmit clock through a clock selector input when the PLL is not locked to the reference clock.

24. (Currently Amended) The upstream multiplexing integrated circuit of claim 14, wherein the ~~reverse clock~~ reverse transmit clock is based on an external oscillator reference clock.

25. (Currently Amended) The upstream multiplexing integrated circuit of ~~claim 19~~ claim 14, further comprising a phase detector that receives a first input from a loop clock and a second input from the voltage controlled oscillator.

26. (Previously Presented) The upstream multiplexing integrated circuit of claim 14, further comprising a Si substrate, and wherein the downstream multiplexing integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second multiplexing integrated circuit comprises integrated circuits formed on a Si substrate.

27. (Currently Amended) A method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprising:

receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first bit rate;

multiplexing the first plurality of bit streams into a second plurality of bit streams at a second bit rate, wherein the second bit rate exceeds the first bit rate;

receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of bit streams is in number;

multiplexing the second plurality of bit streams into the at least one high-speed bit stream having a line bit rate that exceeds the ~~second bit rate; and~~ second bit rate;

generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, wherein the plurality of inputs include a reverse transmit clock generated by the second stage multiplexing integrated circuit; and

producing from the reference clock signal a Phase Locked Loop (PLL) Data Clock having a frequency equal to the second bit rate with a PLL, wherein a plurality of latches receive the PLL Data Clock, latch multiplexed data from the first bit streams, and produce the plurality of second bit streams.

28. (Currently Amended) The method of claim 27 ~~wherein further comprising~~ further comprises:

producing a lock detect signal to indicate when ~~a PLL~~ the PLL is locked to the reference clock signal, wherein a reverse transmit clock is selected as the reference clock signal when the PLL is not locked to the reference clock.

29. (Previously Presented) The method of claim 27, wherein the first plurality of bit streams are received from a communication Application Specific Integrated Circuit (ASIC), and wherein the second stage multiplexing integrated circuit outputs the at least one high speed bit stream to a media interface that produces a media output.

30. (Currently Amended) The method of claim 27, wherein the plurality of inputs ~~comprises~~ include an external oscillator output.

31. (Currently Amended) The method of claim 27, wherein the plurality of inputs ~~further comprises~~ include a voltage-controlled oscillator output.

32. (Currently Amended) The method of claim 27, ~~further comprising the step of~~ further comprises:
selecting the reference clock signal with a ~~clock selector~~ clock selector input.

33. (Cancelled)

34. (Currently Amended) The method of ~~claim 33~~ claim 27, wherein the frequency of ~~PLL Data Clock~~ the PLL Data Clock is 16 times the frequency of the reference clock signal.

35. (Currently Amended) The method of ~~claim 33~~ claim 27, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

36. (Currently Amended) The method of ~~claim 33~~ claim 27, wherein the forward transmit clock is a source centered double data rate clock with respect to the second plurality of bit streams.

37. (Currently Amended) The method of ~~claim 33~~ claim 27, further comprises:
generating a lock detect signal that remains active while the PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference clock signal; and
selecting the ~~reverse clock~~ reverse transmit clock as the reference clock signal through a ~~clock selector~~ clock selector input when the PLL is not locked to the reference clock signal.

38. (Currently Amended) The method of claim 27, wherein the ~~reverse clock~~ reverse transmit clock is based on an external oscillator reference clock.

39. (Currently Amended) The method of ~~claim 33~~ claim 27, further comprises a phase detector that receives a first input from a loop clock and a second input from ~~the voltage controlled oscillator~~ a voltage controlled oscillator.

40. (Currently Amended) The method of ~~claim 33~~ claim 27, further comprises a Si substrate, and wherein the downstream multiplexing integrated circuit includes a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second multiplexing integrated circuit comprises integrated circuits formed on a Si substrate.

41. (Currently Amended) A method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprises:

receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first bit rate;

multiplexing the first plurality of bit streams into a second plurality of bit streams at a second bit rate;

receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate;

multiplexing the second plurality of bit streams into the at least one high-speed bit streams at a line bit rate that exceeds the ~~second bit rate; and~~ second bit rate;

generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, wherein the plurality of inputs include a reverse transmit clock generated by the second stage multiplexing integrated circuit; and

producing a lock detect signal to indicate when a PLL is locked to the reference clock signal, wherein the reverse transmit clock is selected as the reference clock signal when the PLL is not locked to the reference clock.

42. (Cancelled)

43. (New) A method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprising:

receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first bit rate;

multiplexing the first plurality of bit streams into a second plurality of bit streams at a second bit rate, wherein the second bit rate exceeds the first bit rate;

receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of bit streams is in number;

multiplexing the second plurality of bit streams into the at least one high-speed bit stream having a line bit rate that exceeds the second bit rate;

generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, wherein the plurality of inputs include a reverse transmit clock generated by the second stage multiplexing integrated circuit; and

producing a lock detect signal to indicate when a PLL is locked to the reference clock signal, wherein a reverse transmit clock is selected as the reference clock signal when the PLL is not locked to the reference clock.

44. (New) The method of claim 43, wherein the first plurality of bit streams are received from a communication Application Specific Integrated Circuit (ASIC), and wherein the second stage multiplexing integrated circuit outputs the at least one high speed bit stream to a media interface that produces a media output.

45. (New) The method of claim 43, wherein the plurality of inputs include an external oscillator output.

46. (New) The method of claim 43, wherein the plurality of inputs include a voltage-controlled oscillator output.

47. (New) The method of claim 43, further comprises:

selecting the reference clock signal with a clock selector input.

48. (New) The method of claim 43, further comprising:

receiving the reference clock signal and producing a Phase Locked Loop (PLL) Data Clock having a frequency equal to the second bit rate with the PLL, wherein a plurality of latches receive the PLL Data Clock, latch multiplexed data from the first bit streams, and produce the plurality of second bit streams.

49. (New) The method of claim 48, wherein the frequency of the PLL Data Clock is 16 times the frequency of the reference clock signal.

50. (New) The method of claim 48, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

51. (New) The method of claim 48, wherein the forward transmit clock is a source centered double data rate clock with respect to the second plurality of bit streams.

52. (New) The method of claim 43, wherein the reverse transmit clock is based on an external oscillator reference clock.

53. (New) The method of claim 48, further comprises a phase detector that receives a first input from a loop clock and a second input from a voltage controlled oscillator.

54. (New) The method of claim 48, further comprises a Si substrate, and wherein the downstream multiplexing integrated circuit includes a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second multiplexing integrated circuit comprises integrated circuits formed on a Si substrate.